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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,204	SHINOTSUKA ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernández Hernández	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *1-5,12-20 and 27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11 and 21-24* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species 2 (Claims 6-11 and 21-26) in the reply filed on June 1, 2010 is acknowledged. The traversal is on the ground(s) that all claims pertain to a device and method of use, wherein the device is structurally the same in all claims, and the differences in each specie pertains to differences in voltages applied (from external sources) to the gate and/or drain, resulting in different operational states of the device for accomplishing a desired result. This is not found persuasive because although the structure of the device is the same between the Species, the operation performed to said structure is different as discussed in the previous Office Action.

Species 1 is directed to enabling the image sensor to compensate for variations by using a first sensor signal obtainable by setting a gate voltage and a drain voltage of the transistor with shut-off incident light to the photoelectric converting element to normal values when taking video by the image sensor and by using a second sensor signal obtainable by changing the gate voltage and the drain voltage of the transistor to values lower than the normal values when taking video.

Species 2 is different form Species 1 because is directed to enabling the image sensor to previously set a drain voltage of the transistor of each light sensor circuit to a value at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher than a normal value may correspond to a sensor

signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video, and thereafter perform compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video.

Species 3 is different from Species 1 and 2 because is directed to enabling the image sensor to compensate for variations in levels of respective pixel outputs in a dark state and a bright state by using as a dark-state pixel output a sensor signal obtained from each of the light sensor circuits when conducting the transistor with its gate voltage changed to a value higher than a normal value and its drain voltage equal to a normal value for taking video, and by using as a bright-state pixel signal a sensor signal obtainable by changing the drain voltage of the transistor to a value lower than the normal value for taking video.

Species 4 is different form Species 1-3 because is directed to enabling the image sensor to previously set a drain voltage of the transistor to a value at which a sensor signal obtained when conducting the transistor by changing its gate voltage to a value higher than a normal value for taking video may correspond to a sensor signal obtainable in a dark state at a normal gate voltage of the transistor and thereafter to compensate for variations in dark-state output level of each pixel signal by using as the dark-state pixel signal a sensor signal obtainable by changing the gate voltage of the transistor to a value higher than the normal value as a dark-state pixel signal and for variations in bright-state output level of each pixel signal by using as the bright-state

pixel signal a signal obtainable by changing the drain voltage of the transistor to a value lower than the preset value.

Species 5 is different form Species 1-4 because is directed to enabling the image sensor to sample and hold sensor signals read in a time series from respective pixels, obtaining pseudo bright output signals by decreasing by a threshold value the normal drain voltages of the respective transistors corresponding to respective pixels, calculating a difference between each of the obtained pseudo bright output signals and the corresponding sensor signals temporarily stored in the sample-and-hold circuit, and conducting the offset compensation of the previously set bright reference signal by using the determined difference as the offset value.

Species 6 is different form Species 1-5 because is directed to enabling the image sensor to compensate for a variation in each pixel output by using a sensor signal output from the corresponding light sensor circuit by conducting the transistor and changing a drain voltage of the transistor to a higher value or a lower value than the normal value for taking video by the image sensor while maintaining a gate voltage of the transistor at a constant value.

The requirement is still deemed proper and is therefore made FINAL.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on applications filed in Japan on April 27, 2001, September 20, 2001, November 13, 2001 and February 14, 2002 respectively. It is noted, however, that applicant has not filed a

certified copy of the JO 2001-170263, JP 2001-330010, JP 2001-385276 and JP 2002-79681 applications as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-11 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinozuka et al., JP 11-264761 A B1 in view of Chen et al., US Patent 6,618,083 B1.

NOTE: The Examiner has used US Patent 6,909,462 B1 to Shinotsuka et al. as an equivalent English translation of Japanese Patent Publication JP 11-264761 A to Shinozuka et al. in the rejections below. See MPEP 901.05 section III.

5. **Regarding claim 6**, **Shinozuka et al.** disclose an output compensating device of an image sensor (See fig. 5) using a number of light sensor circuits (See fig. 1) each representing a unit pixel and capable of producing in a photoelectric converting element a sensor current proportional to a quantity of light falling thereon and converting the current into a voltage signal by using a sub-threshold region characteristic of a transistor (Fig. 1: QD1) having a logarithmic output characteristic in a weak inverse state and outputting a sensor signal corresponding to the converted voltage signal (See US Patent 6,909,462, col. 7, lines 19-65).

Shinozuka et al. do not explicitly disclose that the output compensating device which provides a means for enabling the image sensor to compensate for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video.

However, **Chen et al.** teach an output compensation device of an image sensor (See fig. 4: 401) using a number of light sensor circuits (See fig. 1) each representing a unit pixel and capable of producing in a photoelectric converting element a sensor signal proportional to a quantity of light falling thereon (Col. 3, lines 44-67), wherein a photodetector (PD) is connected to the source of a reset transistor (RES), the output compensating device further provides a means (charge pump circuit 200 and level shift circuit 204 as shown in fig. 2) for enabling the image sensor to compensate for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video (Chen et al. teach that the gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62)).

Therefore, taking the combined teaching of Shinozuka et al. in view of Chen et al. as a whole, after acknowledging the concept of applying an increased voltage to the gate of the rest transistor to allow the imager to sense the exact drain voltage as taught in Chen et al., it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching Shinozuka et al. to provide a means

for enabling the image sensor to compensate for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video. The motivation to do so would have been to prevent fix pattern noise during the readout operation caused by the mismatch effect of the reset transistor as suggested by Chen et al. (Col. 4, lines 1-62).

6. **Regarding claim 7**, the combined teaching of Shinozuka et al. in view of Chen et al. further teaches that a sensor signal obtainable by changing the gate voltage of the transistor to a value higher than the normal value when taking video corresponds to a sensor signal obtainable in the dark state when taking video (It is noted that in Chen et al., by increasing the gate voltage of the reset transistor, the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received) and is used for offset compensation for variation in the pixel output in the dark state (As discussed in claim 6, Chen et al. further teach that gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state and is used for offset compensation for variation in the pixel output in the dark state as claimed). Grounds for rejecting claim 6 apply here.

The Examiner further noted that the limitations of claim 7 describe how the image sensor is operated, and thus are presented as functional language.

MPEP 2114 states:

> **APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART**
> >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Additionally, MPEP 2114 states the following:

> **MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART**
> A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.).

Therefore, the claim would still be anticipated by the teaching of Shinozuka et al. in view of Chen et al. as Shinozuka et al. has the same structure as that of Applicant's image sensor. If Applicants wish to distinguish over the prior art in terms of

functionality, the Examiner suggests rewriting the claim invoking 112 6th paragraph by using means for language.

7. **Regarding claim 8**, **Shinozuka et al.** discloses an output compensating device of an image sensor (See fig. 5) using a number of light sensor circuits (See fig. 1) each representing a unit pixel and working by producing in a photoelectric converting element a sensor current proportional to a quantity of light falling thereon and converting the current into a voltage signal by using a sub-threshold region characteristic of a transistor (Fig. 1: QD1) having a logarithmic output characteristic in a weak inverse state and outputting a sensor signal corresponding to the converted voltage signal (See US Patent 6,909,462, col. 7, lines 19-65).

Shinozuka et al. do not explicitly disclose that the output compensating device which provides means for enabling the image sensor to previously set a drain voltage of the transistor of each light sensor circuit to a value at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video, and thereafter perform compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video.

However, **Chen et al.** teach an output compensation device of an image sensor (See fig. 4: 401) using a number of light sensor circuits (See fig. 1) each representing a unit pixel and capable of producing in a photoelectric converting element a sensor signal proportional to a quantity of light falling thereon (Col. 3, lines 44-67), wherein a photodetector (PD) is connected to the source of a reset transistor (RES), the output compensating device further provides means (charge pump circuit 200 and level shift circuit 204 as shown in fig. 2, also Chen et al. teaches that chip 400 in fig. 4 also provide supply voltage VDD) for enabling the image sensor to previously set a drain voltage (VDD voltage supplied by the chip 400) of the transistor of each light sensor circuit to a value (i.e. 3.3V, col. 5, lines 4-11) at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher (i.e. 5V, col. 5, lines 4-11) than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video (It is noted that in Chen et al., by increasing the gate voltage of the reset transistor, the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video. See col. 4, lines 1-62), and thereafter (Noting that the increase of the gate voltage occurs while the drain voltage is being applied, which teaches that the increase of the gate voltage occurs after the adjustment of the drain voltage) perform

compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video (Chen et al. teach that the gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62), which teaches thereafter performing compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video as claimed since the gate voltage during capture of the image would be lower than during a reset period to allow the reset transistor to be in a high impedance mode).

Therefore, taking the combined teaching of Shinozuka et al. in view of Chen et al. as a whole, after acknowledging the concept of applying an increased voltage to the gate of the rest transistor to allow the imager to sense the exact drain voltage as taught in Chen et al., it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching Shinozuka et al. to provide means for enabling the image sensor to previously set a drain voltage of the transistor of each light sensor circuit to a value at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video, and thereafter perform

compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video. The motivation to do so would have been to prevent fix pattern noise during the readout operation caused by the mismatch effect of the reset transistor as suggested by Chen et al. (Col. 4, lines 1-62).

8. **Regarding claim 9**, the combined teaching of Shinozuka et al. in view of Chen et al. further teaches that offset compensation for variations in dark-state output levels of pixel signals is performed by using sensor signals obtainable by conducting the transistors with the drain voltage of the preset value and the gate voltage changed to a value higher than the normal value for taking video, which signals correspond to sensor signals obtainable in the dark state for taking video (As discussed in claim 8, Chen et al. further teach that gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase (In which the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received) so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state and is used for offset compensation for variation in the pixel output in the dark state as claimed). Grounds for rejecting claim 8 apply here.

The Examiner further noted that the limitations of claim 9 describe how the image sensor is operated, and thus are presented as functional language.

MPEP 2114 states:

APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART

>While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Additionally, MPEP 2114 states the following:

MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.).

Therefore, the claim would still be anticipated by the teaching of Shinozuka et al. in view of Chen et al. as Shinozuka et al. has the same structure as that of Applicant's

image sensor. If Applicants wish to distinguish over the prior art in terms of functionality, the Examiner suggests rewriting the claim invoking 112 6th paragraph by using means for language.

9. **Regarding claims 10 and 11**, similar to claim 9, the limitations of claims 10 and 11 describe how the image sensor is operated, and thus are presented as functional language.

MPEP 2114 states:

> **APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART**
> >While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

Additionally, MPEP 2114 states the following:

> **MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART**
> A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The

Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.).

Therefore, although the prior art of record does not teach the described functionalities of claims 10 and 11, claims 10 and 11 are anticipated by the teaching of Shinozuka et al. in view of Chen et al. as Shinozuka et al. has the same structure as that of Applicant's image sensor. If Applicants wish to distinguish over the prior art in terms of functionality, the Examiner suggests rewriting the claims invoking 112 6th paragraph by using means for language.

10. **Regarding claim 21**, Shinozuka et al. disclose a method of compensating for the outputs of a number of light sensor circuits (See fig. 1) of an image sensor (See fig. 5), each light sensor circuit representing a unit pixel and capable of producing in a photoelectric converting element a sensor current proportional to a quantity of light falling thereon and converting the current into a voltage signal by using a sub-threshold region characteristic of a transistor (Fig. 1: QD1) having a logarithmic output characteristic in a weak inverse state and outputting a sensor signal corresponding to the converted voltage signal (See US Patent 6,909,462, col. 7, lines 19-65).

Shinozuka et al. do not explicitly disclose the steps of compensating for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video.

However, **Chen et al.** teach an output compensation device and method for an image sensor (See fig. 4: 401) using a number of light sensor circuits (See fig. 1) each

representing a unit pixel and capable of producing in a photoelectric converting element a sensor signal proportional to a quantity of light falling thereon (Col. 3, lines 44-67), wherein a photodetector (PD) is connected to the source of a reset transistor (RES), the output compensating device further provides a means (charge pump circuit 200 and level shift circuit 204 as shown in fig. 2) for enabling the image sensor to compensate for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video (Chen et al. teach that the gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62)).

Therefore, taking the combined teaching of Shinozuka et al. in view of Chen et al. as a whole, after acknowledging the concept of applying an increased voltage to the gate of the rest transistor to allow the imager to sense the exact drain voltage as taught in Chen et al., it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching Shinozuka et al. to provide the steps of compensating for variations in each pixel output by using a sensor signal obtained by conducting the transistor by changing its gate voltage to a value higher than normal values when taking video. The motivation to do so would have been to prevent fix pattern noise during the readout operation caused by the mismatch effect of the reset transistor as suggested by Chen et al. (Col. 4, lines 1-62).

11. **Regarding claim 22**, the combined teaching of Shinozuka et al. in view of Chen et al. further teaches that a sensor signal obtainable by changing the gate voltage of the transistor to a value higher than the normal value when taking video corresponds to a sensor signal obtainable in the dark state when taking video (It is noted that in Chen et al., by increasing the gate voltage of the reset transistor, the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received) and is used for offset compensation for variation in the pixel output in the dark state (As discussed in claim 21, Chen et al. further teach that gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state and is used for offset compensation for variation in the pixel output in the dark state as claimed). Grounds for rejecting claim 21 apply here.

12. **Regarding claim 23**, **Shinozuka et al.** disclose a method of compensating for the outputs of a number of light sensor circuits (See fig. 1) of an image sensor (See fig. 5), each light sensor circuit representing a unit pixel and working by producing in a photoelectric converting element a sensor current proportional to a quantity of light falling thereon and converting the current into a voltage signal by using a sub-threshold region characteristic of a transistor (Fig. 1: QD1) having a logarithmic output

characteristic in a weak inverse state and outputting a sensor signal corresponding to the converted voltage signal (See US Patent 6,909,462, col. 7, lines 19-65).

Shinozuka et al. do not explicitly disclose the steps of previously setting a drain voltage of the transistor of each light sensor circuit to a value at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video, and thereafter performing compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video.

However, **Chen et al.** teach an output compensation device and method for an image sensor (See fig. 4: 401) using a number of light sensor circuits (See fig. 1) each representing a unit pixel and capable of producing in a photoelectric converting element a sensor signal proportional to a quantity of light falling thereon (Col. 3, lines 44-67), wherein a photodetector (PD) is connected to the source of a reset transistor (RES), the output compensating device further provides means (charge pump circuit 200 and level shift circuit 204 as shown in fig. 2, also Chen et al. teaches that chip 400 in fig. 4 also provide supply voltage VDD) for enabling the image sensor to previously set a drain voltage (VDD voltage supplied by the chip 400) of the transistor of each light sensor circuit to a value (i.e. 3.3V, col. 5, lines 4-11) at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher (i.e. 5V, col. 5,

lines 4-11) than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video (It is noted that in Chen et al., by increasing the gate voltage of the reset transistor, the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video. See col. 4, lines 1-62), and thereafter (Noting that the increase of the gate voltage occurs while the drain voltage is being applied, which teaches that the increase of the gate voltage occurs after the adjustment of the drain voltage) perform compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video (Chen et al. teach that the gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62), which teaches thereafter performing compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video as claimed since the gate voltage during capture of the

image would be lower than during a reset period to allow the reset transistor to be in a high impedance mode).

Therefore, taking the combined teaching of Shinozuka et al. in view of Chen et al. as a whole, after acknowledging the concept of applying an increased voltage to the gate of the rest transistor to allow the imager to sense the exact drain voltage as taught in Chen et al., it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching Shinozuka et al. to provide the steps of previously setting a drain voltage of the transistor of each light sensor circuit to a value at which a sensor signal obtained by conducting the transistor with its gate voltage changed to a value higher than a normal value may correspond to a sensor signal obtainable in a dark state of the light sensor circuit with the normal gate voltage of the transistor when taking video, and thereafter performing compensation for variations in output of each pixel signal by using a sensor signal obtainable from the light sensor circuit by changing the gate voltage of the transistor with the preset drain voltage to a value higher than the normal value for taking video. The motivation to do so would have been to prevent fix pattern noise during the readout operation caused by the mismatch effect of the reset transistor as suggested by Chen et al. (Col. 4, lines 1-62).

13. **Regarding claim 24**, the combined teaching of Shinozuka et al. in view of Chen et al. further teaches that offset compensation for variations in dark-state output levels of pixel signals is performed by using sensor signals obtainable by conducting the

transistors with the drain voltage of the preset value and the gate voltage changed to a value higher than the normal value for taking video, which signals correspond to sensor signals obtainable in the dark state for taking video (As discussed in claim 23, Chen et al. further teach that gate voltage is increased to allow the imager to sense the same exact drain voltage during the reset phase (In which the generated signal would correspond to sensor signal obtainable in the dark state when taking video since the signal generated is the same signal as the drain voltage which would represent the amount of signal when no light is received) so that mismatch effect of the reset transistor will not produce fix pattern noise during the readout operation (Col. 4, lines 1-62). This teaches that the signal which corresponds to a sensor signal obtainable in a dark state and is used for offset compensation for variation in the pixel output in the dark state as claimed). Grounds for rejecting claim 23 apply here.

Allowable Subject Matter

14. **Claims 25 and 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

16. **Regarding claim 25**, the main reason for indication of allowable subject matter is because the prior art of record fails to teach or reasonably suggest that gain-compensation for variations in bright-state output levels of pixel signals is performed by

using sensor signals obtainable by changing the gate voltage and the drain voltage of the transistor with shut-off incident light to the photoelectric converting element to values lower than the normal values for taking video, which signals correspond to sensor signals obtainable in a bright state for taking video, including all the limitations of claims 23 and 24.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. US Patent 6,140,630 to Rhodes which appears to teach a similar approach to reduce variations in each pixel by increasing the gate voltage so that the voltage drop across the reset transistor does not lower the VDD reset charge (See col. 5, line 59 – col. 6, line 17).

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernández Hernández whose telephone number is (571)272-7311. The examiner can normally be reached on 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Nelson D. Hernández Hernández/
Examiner, Art Unit 2622
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